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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,371	03/04/2002	Dawei Huang	HUANG 2-1 (58655)	5175

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,371	HUANG ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 1-22 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites, "a data receiving circuit for receiving a digital input data sequence and periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length", which has a multitude of interpretations, for example: 1) --a data receiving circuit for receiving a digital input data sequence **based on a constraint length** and periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence --, 2) --**a data receiving circuit for periodically inserting known symbols into a received digital input data sequence based on a constraint length** and forming an expanded digital input data sequence --, 3) --a data receiving circuit for receiving a digital input data sequence and periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence **whereby the expanded digital input data sequence is** based on a constraint length--, etc. That is, it is not clear which of the clauses or which combination of the cluases a) "receiving a digital input data sequence", b) "periodically inserting known symbols into the digital input data sequence" or c) "forming an expanded digital input data sequence" that the term "based on a constraint length" modifies.

For now, in the interest of speeding up prosecution, the Examiner examines the Application based on the following two interpretations: 3) --a data receiving circuit for receiving a digital input data sequence and periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence **whereby the expanded digital input data sequence is** based on a constraint length--. If the Applicant believes that any other interpretation is warranted, the Examiner suggests that the Applicant amend so that the Examiner can do the appropriated search for the particular interpretation that the Applicant wants examined.

Claim 10 recites, "periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length", which has similar problems as in claim 1.

For now, in the interest of speeding up prosecution, the Examiner examines the Application based on the following two interpretations: 3) -- periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence **whereby the expanded digital input data sequence is** based on a constraint length--.

Claim 17 recites, "periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length k=m-1", which has similar problems as in claim 1.

For now, in the interest of speeding up prosecution, the Examiner examines the Application based on the following two interpretations: 3) -- periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence **whereby the expanded digital input data sequence is** based on a constraint length k=m-1--.

Claim 17 recites, "a code rate is R=1/l". The letter l in the term "R=1/l" is undefined.

Claim 1 recites, "an encoder operatively connected to said data receiving circuit for trellis encoding the expanded digital input data sequence to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis are reduced".

The Examiner asserts that a Trellis is generally a state diagram that is expanded timewise according to a state machine used to generate a code. All of the connections in the state diagram are required to generate the code. However during decoding not all of the connections in the time-wise expanded state machine called the Trellis are required for decoding the code and various connections can be ignored especially in the case that values within the Trellis are already known since a path for determining the codeword in question must pass through a known value at a particular time and cannot pass through any other value at that particular time. However a Trellis is still just a state machine expanded in time whereby all the connections in the state diagram still exist in the Trellis whether a decoder chooses to use or ignore connections or not. The

Examiner asserts that the implementation of a Trellis is a function of a decoder and not the function of an encoder.

The Examiner assumes the Applicant intended --an encoder operatively connected to said data receiving circuit for trellis encoding the expanded digital input data sequence to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis **may be ignored by a decoder at a receiving end**--.

Claim 10 recites, "trellis encoding the expanded digital input data sequence based on the constraint length to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis are reduced".

The Examiner assumes the Applicant intended --trellis encoding the expanded digital input data sequence based on the constraint length to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis **may be ignored by a decoder at a receiving end**--.

Claim 17 recites, "trellis encoding the expanded digital input data sequence to produce a channel coded data stream, wherein the number of connections between trellis nodes in a trellis are reduced".

The Examiner assumes the Applicant intended --trellis encoding the expanded digital input data sequence to produce a channel coded data stream, wherein the number of connections between trellis nodes in a trellis **may be ignored by a decoder at a receiving end**--.

Claims 8 and 9 fail to further limit the "system for channel coding data" in claim 1 decoders are not used in encoding data. Claims 8 and 9 appear to be an attempt to claim another invention.

Claim 10 recites, "A method for channel coding data within a digital communications system". Claims 15 and 16 fail to further limit the "method for channel coding data" in claim 10 decoders are not used in encoding data. Claims 8 and 9 appear to be an attempt to claim another invention.

Claim 17 recites, "A method for channel coding data within a digital communications system". Claims 20 and 21 fail to further limit the "method for channel coding data" in claim 17 decoders are not used in encoding data. Claims 20 and 21 appear to be an attempt to claim another invention.

Claims 3, 12 and 19 recite, "the inserted zeros comprise an equivalent time varying convolutional code". The IEEE Authoritative Dictionary of IEEE Standards Terms defines code 1) a set of rules to convert data from one form of representation to another or 2) a character or bit pattern that is assigned a particular meaning. A group of inserted zeros is not a set of rules to convert data from one form of representation to another nor has the Applicant taught anywhere in the Applicant's specification that a group of inserted zeros is assigned a particular meaning.

The Examiner assumes the Applicant intended zeros are inserted prior to convolutional coding the expanded digital input data sequence.

Claim Objections

2. Claims 8, 9, 15 and 16 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 1 recites, "A system for channel coding data within a digital communications system". Claims 8 and 9 fail to further limit the "system for channel coding data" in claim 1 decoders are not used in encoding data. Claims 8 and 9 appear to be an attempt to claim another invention.

Claim 10 recites, "A method for channel coding data within a digital communications system". Claims 15 and 16 fail to further limit the "method for channel coding data" in claim 10 decoders are not used in encoding data. Claims 8 and 9 appear to be an attempt to claim another invention.

Claim 17 recites, "A method for channel coding data within a digital communications system". Claims 20 and 21 fail to further limit the "method for channel coding data" in claim 17 decoders are not used in encoding data. Claims 20 and 21 appear to be an attempt to claim another invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5 and 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Simanapalli; Sivanand (US 6081921 A).

35 U.S.C. 102(b) rejection of claims 1, 4 and 10.

Simanapalli teaches a data receiving circuit for receiving a digital input data sequence and periodically inserting known symbols into the digital input data sequence (Figure 2 in Simanapalli teaches Convolutional Encoder 22, which receives frame 18 and periodically inserts known zero bit symbols every 2 bits; Note: col. 3, lines 10-15 in Simanapalli teaches that a 0 is inserted into every other position of the sequence [b_{15}, b_{14},..., b_2, b_1, b_0, b_{-1},..., b_{-4}]) and forming an expanded digital input data sequence based on a constraint length (col. 1, lines 45-46 in Simanapalli teaches that N is he constraint length of the convolutional code; col. 2, lines 1-5 in Simanapalli teaches that N=4 are the 4 past bits [b_{-1}, b_{-2}, b_{-3}, b_{-4}] in [b_{15}, b_{14},..., b_2, b_1, b_0, b_{-1},..., b_{-4}], hence the expanded digital input data sequence [b_{15}, 0, b_{14}, 0,..., b_2, 0, b_1, 0, b_0, 0, b_{-1}, 0,..., b_{-4}, 0] is still based on the constraint length N=4 since the original sequence [b_{15}, b_{14},..., b_2, b_1, b_0, b_{-1},..., b_{-4}] is based on the constraint length N=4); and an encoder operatively connected to said data receiving circuit for trellis encoding the expanded digital input data sequence to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis **may be ignored by a decoder at a receiving end**, said encoder operative according to the constraint length (since half of

the values of the expanded digital input data sequence [b_{15}, 0, b_{14}, 0,..., b_2, 0, b_1, 0, b_0, 0, b_{-1}, 0,..., b_{-4}, 0] in col. 3, lines 10-15 in Simanapalli are known the path must pass through a 0 value at that time in the Trellis which clearly allows for reduction of the necessary calculations on a Trellis at a decoder at the receiving end).

35 U.S.C. 102(b) rejection of claims 2, 3, 11 and 12.

The Abstract in Kato teaches that the inserted bit can be a one or a zero.

35 U.S.C. 102(b) rejection of claims 5 and 13.

Convolutionally coded codewords are inherently in a one-to-one mapping with the distinct paths on a trellis to binary sequences.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 8, 9, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simanapalli; Sivanand (US 6081921 A) in view of Kato; Osamu et al. (US 5436918 A, hereafter referred to as Kato).

35 U.S.C. 103(a) rejection of claims 8, 9, 15 and 16.

Simanapalli substantially teaches the claimed invention described in claims 1-5 and 10-13 (as rejected above).

However Simanapalli does not explicitly teach the specific use of a Viterbi decoder.

Kato, in an analogous art, teaches use of a Viterbi decoder (Col. 1, lines 25-31 in Kato teach a Maximum Likelihood (ML) decoder comprising a Viterbi decoder).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Simanapalli with the teachings of Kato by including use of a Viterbi decoder. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a Viterbi decoder would have provided one of the most prevalent and common means for decoding a convolutional code.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JOSEPH TORRES
PRIMARY EXAMINER

Joseph D. Torres, PhD
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Art Unit 2133